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| Instructions | Info | Dev / Introduced /  ( 1st CPU with that feature) |
| MMX | ***M****ulti-****M****edia* ***Ex****tension.* | 1990’s /  Jan 8, 1997  [Pentium P5 “with MMX” CPUs] |
| SSE | ***S****treaming* ***S****IMD\** ***E****xtensions is a major x86 extension*  *\*****SIMD*** *(****S****ingle* ***I****nstruction,* ***M****ultiple* ***D****ata) architecture set.* | xxxx / 1999  [in Pentium 3 CPUs] |
| SSE*2* | *One of* ***SIMD*** *supplementary instruction.*  *Major features:*  *- double-precision (64bit) floating point for all SSE operations;*  *- MMX integer operations on 128bit XMM registers;* | xxxx / 2000  [in Pentium 4 CPUs] |
| SSE*3* | *Code name* ***P****rescott* ***N****ew* ***I****nstructions [PNI] instruction set of IA-32(x86) architecture.*  *- DSP math instructions;*  *- thread management instructions;*  *- allowing to addition/multiplication of two numbers that are stored in the same register;* | Early 2004’s  [in “**Prescott**” rev. of Pentium 4 CPUs] |
| SSSE*3* | *The 4th extension of supplemental SSE3.*  *- 16 new instructions which include permuting the bytes in a word;*  *- multiplying 16bit fixed-point numbers with correct roundings;*  *- within-word accumulate instructions;* | xxxx /  June 26, 2006  [in Xeon “**Woodcrest**” CPUs] |
| SSSE*4.1* | *47 new instructions that execute operations which are not specific to multimedia applications. Several of those are enabled by single-cycle shuffle engine Penryn (shuffle operations reorder bytes within a register).* | xxxx / Sept 27, 2006  & spring of 2007.  (Intel Core 2 “**Penryn**” CPUs) |
| SSSE*4.2* | *Added STTNI (****S****tring and* ***T****ext* ***N****ew* ***I****nstructions) several new instructions that perform character searches and comparison on two operations on two operands of 16bytes at a time. Also added CRC32 instruction to compute cyclic redundancy checks as used in certain data transfer protocol.* | Jul 27, 2006 (Nehalem);  Jun 1, 2013  (Haswell);  (Intel Core 1st gen “**Nehalem**” &  Intel Core 4th gen “**Haswell**” CPUs) |
| EM64T | *The 64bit version of x86 instruction set enhances server and workstation platforms with 64 bit addressability and related instructions.*  *- New modes of operation;*  *- 4-level paging mode;*  *- expanded general-purpose registers to 64bit;*  *- modified instructions to support 64bit operands & 64bit addressing mode;*  *- compatibility mode defined in the architecture allows 16bit & 32bit user applications;* | xxxx /  Mar 2004  officially named “**EM64T**”;  Jun 2004  (Xeon “**Nocona**” CPUs);  Feb 14, 2005  (Xeon “**Irwindale**” CPUs); |
| VT-x | *Virtualization Technology.*  *- Allows the PC user enable hardware virtualization support at the CPU level.* | xxxx /  Nov 13, 2005  (Pentium 4 **662** & **672** CPUs) |
| AES | ***A****dvanced* ***E****ncryption* ***S****tandard instruction set.*  *- Improve the speed and security of applications performing encryption and decryption.* | **Jan 7 2010**  (Core i7 1st gen “**Gulftown**” CPUs) |
| AVX | ***A****dvanced* ***V****ector* ***E****xtension is a 256bit point vector extension of IA SIMD.*  *- SIMD registers is increased from 128bits to 256 bits;*  *- includes an extension for both instructions and registration set;* | **xxxx /**  **Mar 2008;**  **Jan 9 2011**  (“**Sandy Bridge**” CPUs) |

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| AVX*2* | *aka Haswell New Instructions. An Expansion of AVX instruction set.*  *- expansion of most vector integer SSE & AVX instructions to 256bit;*  *- gather/scatter support enabling vector elements to be loaded from non-contiguous memory locations;*  *- DWORD and QWORD-granularity any-to-any permutes;*  *- vector shifts;* | xxxx /  Jun 2013  (Core i7 4th  gen “**Haswell**” & “**Xeon**” CPUs) |
| FMA*3* | ***F****used* ***M****ultiply-****A****dd is an extension to the 128 and 256bit SSE instructions in the x86 microprocessor instruction set to perform fused multiply-add operations.* | xxxx / 2013  (Core i7 4th gen“**Haswell**” CPU  **except** Pentium & Celeron CPUs) |
| TSX | ***T****ransactional* ***S****ync* ***Ex****tension (TSX-IN) is an extension to the x86 instruction set architecture.*  *- adds hardware transactional memory support;*  *- speeding up execution of multi-threaded software;* | Feb 2012 (announced)  / Jun 2013 (debuted)    Aug 2014  (Core i3, i5, i7 4th gen “**Haswell**” **except** **below** **45xx**/**45xxK** / **45xxR** CPUs) |